Abstract of the Disclosure

A divider of a DLL(delay locked loop) measures tAC for various periods due to variation of process, temperature and a supply voltage and provides a divided clock having an optimum tAC. The clock divider includes a clock dividing unit, a test mode clock providing unit and a normal mode clock providing unit. The clock dividing unit receives a source clock of the DLL to generate a plurality of divided clocks, each having a period different from each other. The test mode clock providing unit selectively outputs the plurality of the divided clocks in a test mode in response to a test mode signal and a test mode period selecting signal. And, the normal mode clock providing unit outputs selected one of the plurality of the divided clocks in a normal mode in response to the test mode signal.